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1 **Distributed Electrical Power Management Architecture**
Bailey, M.; Hale, N.; Ucerpi, G.; Hunt, J.-A.; Mollov, S.; Forsyth, A.;
Electrical Machines and Systems for the More Electric Aircraft (Ref. No. 1999/ IEE Colloquium on , 9 Nov. 1999
Pages:7/1 - 7/4

[Abstract] [PDF Full-Text (252 KB)] **IEE CNF**

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2 **Power distribution system design methodology and capacitor select for modern CMOS technology**
Smith, L.D.; Anderson, R.E.; Forehand, D.W.; Pelc, T.J.; Roy, T.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 22 , Issue: 3 , Aug. 1999
Pages:284 - 291

[Abstract] [PDF Full-Text (204 KB)] **IEEE JNL**

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3 **Modeling, simulation, and measurement of mid-frequency simultane switching noise in computer systems**
Becker, W.D.; Eckhardt, J.; Frech, R.W.; Katopis, G.A.; Klink, E.; McAllister, M McNamara, T.G.; Muench, P.; Richter, S.R.; Smith, H.;
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on] , Volume: 21 , Issue: 2 , Ma 1998
Pages:157 - 163

[Abstract] [PDF Full-Text (136 KB)] **IEEE JNL**

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4 **Mid-frequency simultaneous switching noise in computer systems**
Becker, W.; Smith, H.; McNamara, T.; Muench, P.; Eckhardt, J.; McAllister, M Katopis, G.; Richter, S.; Frech, R.; Klink, E.;

Electronic Components and Technology Conference, 1997. Proceedings., 47th
21 May 1997
Pages:676 - 681

[Abstract] [PDF Full-Text (600 KB)] IEEE CNF

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5 **Power distribution system for JEDEC DDR2 memory DIMM**
Smith, L.D.; Lee, J.;
Electrical Performance of Electronic Packaging, 2003 , 27-29 Oct. 2003
Pages:121 - 124

[Abstract] [PDF Full-Text (343 KB)] IEEE CNF

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6 **Model to hardware correlation for power distribution induced I/O n in a functioning computer system**
Sungjun Chun; Smith, L.; Anderson, R.; Swaminathan, M.;
Electronic Components and Technology Conference, 2002. Proceedings. 52nd
31 May 2002
Pages:319 - 324

[Abstract] [PDF Full-Text (543 KB)] IEEE CNF

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7 **An application of a protective relaying scheme over an ethernet LAN/WAN**
Brunello, G.; Smith, R.; Campbell, C.B.;
Transmission and Distribution Conference and Exposition, 2001
IEEE/PES , Volume: 1 , 28 Oct.-2 Nov. 2001
Pages:522 - 526 vol.1

[Abstract] [PDF Full-Text (239 KB)] IEEE CNF

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8 **A transmission-line model for ceramic capacitors for CAD tools base measured parameters**
Smith, L.D.; Hockanson, D.; Kothari, K.;
Electronic Components and Technology Conference, 2002. Proceedings. 52nd
31 May 2002
Pages:331 - 336

[Abstract] [PDF Full-Text (638 KB)] IEEE CNF

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9 **Distributed SPICE circuit model for ceramic capacitors**
Smith, L.D.; Hockanson, D.;
Electronic Components and Technology Conference, 2001. Proceedings., 51st
May-1 June 2001
Pages:523 - 528

[Abstract] [PDF Full-Text (324 KB)] IEEE CNF

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1 **Design oriented analysis of package power distribution system considering target impedance for high performance microprocessors**
Mandhana, O.P.;
Electrical Performance of Electronic Packaging, 2001 , 29-31 Oct. 2001
Pages:273 - 276

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

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2 **Modeling, Analysis and Design of Resonant Free Power Distribution Network for Modern Microprocessor Systems**
Mandhana, O.P.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 27 , Issue: 1 , Feb. 2004
Pages:107 - 120

[Abstract] [PDF Full-Text (1256 KB)] **IEEE JNL**

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3 **Modeling and analysis of power distribution networks for Gigabit applications**
Jinwoo Choi; Sung-Hwan Min; Joong-Ho Kim; Swaminathan, M.; Beyene, W.; Xingchao Yuan;
Mobile Computing, IEEE Transactions on , Volume: 2 , Issue: 4 , Oct.-Dec. 20
Pages:299 - 313

2003

[Abstract] [PDF Full-Text (1917 KB)] **IEEE JNL**

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4 **A simple finite-difference frequency-domain (FDFD) algorithm for analysis of switching noise in printed circuit boards and packages**
Ramahi, O.M.; Subramanian, V.; Archambeault, B.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 26 , Issue: 2 , May 2003

Pages:191 - 198

[Abstract] [PDF Full-Text (2996 KB)] IEEE JNL

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5 **Modeling of multilayered power distribution planes using transmiss matrix method**
Joong-Ho Kim; Swaminathan, M.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 25 , Issue: 2 , May 2002
Pages:189 - 199

[Abstract] [PDF Full-Text (682 KB)] IEEE JNL

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6 **Modeling and transient simulation of planes in electronic packages**
Nanju Na; Jinseong Choi; Sungjun Chun; Madhavan Swaminathan; Jegannath Srinivasan;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 23 , Issue: 3 , Aug. 2000
Pages:340 - 352

[Abstract] [PDF Full-Text (364 KB)] IEEE JNL

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7 **Power distribution system design methodology and capacitor select for modern CMOS technology**
Smith, L.D.; Anderson, R.E.; Forehand, D.W.; Pelc, T.J.; Roy, T.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 22 , Issue: 3 , Aug. 1999
Pages:284 - 291

[Abstract] [PDF Full-Text (204 KB)] IEEE JNL

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8 **Analysis and design of critically damped power distribution network high performance microprocessor systems**
Mandhana, O.P.;
Electrical Performance of Electronic Packaging, 2002 , 21-23 Oct. 2002
Pages:183 - 186

[Abstract] [PDF Full-Text (425 KB)] IEEE CNF

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9 **Model to hardware correlation for power distribution induced I/O n in a functioning computer system**
Sungjun Chun; Smith, L.; Anderson, R.; Swaminathan, M.;
Electronic Components and Technology Conference, 2002. Proceedings. 52nd 31 May 2002
Pages:319 - 324

[Abstract] [PDF Full-Text (543 KB)] IEEE CNF

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8033117, B2004-08-1265F-081, C2004-08-5130-063; 20040718.

Title
Optimizing the output **impedance** of a **power** delivery network for microprocessor systems.

Author(s)
Mandhana-O-P.

Author affiliation
Somerset Design Center, Motorola Inc, Austin, TX, USA.

Source
2004 Proceedings. 54th Electronic Components and Technology Conference, Vol.2, Las Vegas, NV, USA, 1-4 June 2004.
In: p.1975-82 Vol.2, 2004.

ISSN
ISBN: 0-7803-8365-6, CCCC: 0-7803-8365-6/04/ ($20.00).

Publication year
2004.

Language
EN.

Publication type
CPP Conference Paper.

Treatment codes
P Practical.

Abstract
This paper presents a systematic design oriented frequency domain analysis of a multi-stage **power distribution** network. (PDN) of a microprocessor system with the **power** source represented as, a close-loop small-signal **model** of a dc to dc, converter. Generalized analytical expressions are derived for the output **impedance** including voltage sensing at different, stages. of, the multistage PDN. The affect of optimally selecting the ESR, ESL and capacitance of the **decoupling capacitors** at different stages of the PDN is described in terms of the converter's loop gain, crossover frequency, phase margin and their impact on realizing the flat output **impedance** at the microprocessor core. **Simulation** results are presented to support the validity of the novel design oriented analysis. (8 refs).

Descriptors
DC-DC-power-convertors; electric-impedance; equivalent-circuits; frequency-domain-analysis; lumped-parameter-networks; microprocessor-chips; power-supply-circuits; transfer-functions.

Keywords
multistage **power distribution** network; microprocessor system; design oriented frequency domain analysis; output **impedance; power** delivery network; close loop small signal **model;** DC DC converter; **decoupling capacitors;** loop gain; crossover frequency; phase margin; **power** integrity;

lumped equivalent **model.**

Classification codes

B1265F (Microprocessors and microcomputers).
B1210 (**Power** electronics, supply and supervisory circuits).
B1130 (General circuit analysis and synthesis methods).
C5130 (Microprocessor chips).
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INSPEC - 1969 to date (INZZ)

Accession number & update
7582312, B2003-05-1265F-017; 20030414.

Title
Analysis and design of critically damped **power distribution** network for high performance microprocessor systems.

Author(s)
Mandhana-O-P.

Author affiliation
Somerset Design Center, Motorola Corp, Austin, TX, USA.

Source
IEEE 11th Topical Meeting on Electrical Performance of Electronic Packaging, Monterey, CA, USA, 21-23 Oct. 2002.
Sponsors: IEEE Microwave Theory & Techniques Soc., IEEE Components, Packaging & Manuf. Technol. Soc.
In: p.183-6, 2002.

ISSN
ISBN: 0-7803-7451-7, CCCC: 0-7803-7451-7/02/ ($17.00).

Publication year
2002.

Language
EN.

Publication type
CPP Conference Paper.

Treatment codes
T Theoretical or Mathematical.

Abstract
Based on the design oriented time domain and frequency analysis of the lumped **model** of **power distribution** network (PDN) involving high performance microprocessor core, packaging, PCB and **power** source, this paper presents simple design equations to realize the critically damped transient response at the microprocessor load. In order to realize the critically damped PDN with flat output **impedance** magnitude, a systematic method of sizing the **decoupling capacitors** to be used in the distributed **model** of PDN is described. **Simulation** results are presented, verifying the validity of the systematic design methodology. (4 refs).

Descriptors
frequency-domain-analysis; integrated-circuit-packaging; microcomputers; microprocessor-chips; network-analysis; network-synthesis; power-supply-circuits; time-domain-analysis; transient-response.

Keywords
critically damped **power distribution** network; high performance microprocessor systems; design

oriented time domain analysis; design oriented frequency domain analysis; lumped **model;** packaging; PCB; **power** source; design equations; critically damped transient response; flat output **impedance** magnitude; **decoupling** capacitor sizing; distributed **model;** design methodology.

Classification codes

B1265F (Microprocessors and microcomputers).
B1210 (**Power** electronics, supply and supervisory circuits).
B0170J (Product packaging).
B1130 (General circuit analysis and synthesis methods).

Terms used
power distribution and **decoupling capacitors** and **simulation** and **model** and **impedance** and **rung** and **capac**

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1 Power distribution issues: Macro-modeling concepts for the chip electrical interface

Brian W. Amick, Claude R. Gauthier, Dean Liu

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(515.95 KB) Additional Information: full citation, abstract, references, index terms

The power delivery network is made up of passive elements in the distribution network, as well as transistor loads. A chip typically has three types of power supplies that require attention: core, I/O Core circuits consist of digital circuits and have the largest current demand. In addition to all of th issues/models for the core, modeling the I/O subsystem has the additional requirement of modelin paths and discontinuities. The analog circuits present yet ...

Keywords: VLSI power distribution, analog and I/O power delivery, high speed microprocessor d inductance

2 Session 10C: Embedded tutorial: IC power distribution challenges: IC power distribution cha

Sudhakar Bobba, Tyler Thorp, Kathirgamar Aingaran, Dean Liu

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aid**

Full text available: pdf(125.96 KB) Additional Information: full citation, abstract, references, citings, index term

With each technology generation, delivering a timevarying current with reduced nominal supply vo variation is becoming more difficult due to increasing current and power requirements. The power network design becomes much more complex and requires accurate analysis and optimizations at abstraction in order to meet the specifications. In this paper, we describe techniques for estimatio supply voltage variations that can be used in the design of the power delive ...

3 Modeling of Multi-Layered Power Distribution Planes Including Via Effects Using Transmissio Method

Joong-Ho Kim, Erdem Matoglu, Jinwoo Choi, Madhavan Swaminathan

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/V**

Full text available: pdf(259.07 KB) Publisher Site Additional Information: full citation, abstract

This paper presents a method for analyzing multi-layered power distribution networks in the frequ domain.Using a two dimensional array of distributed RLCG circuits,multi-layered power distributio represented.Each plane pair is connected by vias, which are modeled as partial self and mutual in the efficient computation of the power distribution impedances at specific points in the network,a and multi-output transmission matrix method has been used, which is ...

4 Electromagnetic modeling and signal integrity simulation of power/ground networks in high s packages and printed circuit boards
Frank Y. Yuan
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(275.46 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

The electromagnetic modeling and parameter extraction of digital packages and PCB boards for sy integrity applications are presented. A systematic approach to analyze complex power/ground stru simulate their effects on digital systems is developed. First, an integral equation boundary elemen applied to the electromagnetic modeling of the PCB structures. Then, equivalent circuits of the pow networks are extracted from the EM solution. In an integra ...

Keywords: custom sizing, migration, timing optimazation

5 Power supply noise analysis methodology for deep-submicron VLSI chip design
Howard H. Chen, David D. Ling
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(237.07 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index term

This paper describes a new design methodology to analyzethe on-chip power supply noise for high microprocessors.Based on an integrated package-level andchip-level power bus model, and a simu switching circuitmodel for each functional block, this methodology offersthe most complete and ac analysis of Vdd distributionfor the entire chip. The analysis results not only providedesigners with ¿I noise and the resistive IRdrop data at the same time, but also allow d ...

6 Interconnect parasitic extraction in the digital IC design methodology
Mattan Kamon, Steve McCormick, Ken Sheperd
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aid**

Full text available: pdf(129.08 KB) Additional Information: full citation, abstract, references, citings, index term

Accurate interconnect analysis has become essential not only for post-layout verification but also This tutorial explores interconnect analysis and extraction methodology on three levels: coarse ex guide synthesis, detailed extraction for full-chip analysis, and full 3D analysis for critical nets. We describe the electrical issues caused by parasitics and how they have, and will be, influenced by c technology. The importance of model order ...

7 Session 10A: power analysis and optimization: Simulation and optimization of the power dist network in VLSI circuits
G. Bai, S. Bobba, I. N. Hajj
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aid**

Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings

In this paper, we present simulation techniques to estimate the worst-case voltage variation using for the power distribution network. Pattern independent maximum envelope currents are used as input for performing the frequency-domain steady-state simulation of the linear RC circuit to evalu worst-case instantaneous voltage drop for the RC power distribution networks. The proposed tech existing techniques, is guaranteed to give the maximum voltage drop at ...

8 Session 10C: Embedded tutorial: IC power distribution challenges: Challenges in power-gro
Shen Lin, Norman Chang
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aid**

Full text available: pdf(54.74 KB) Additional Information: full citation, abstract, references, citings, index term

With the advance of semiconductor manufacturing, EDA, and VLSI design technologies, circuits wi increasingly higher speed are being integrated at an increasingly higher density. This trend causes

correspondingly larger voltage fluctuations in the on-chip power distribution network due to IR-dro noise, or LC resonance. Therefore, Power-Ground integrity becomes a serious challenge in designi high-performance circuits. In this paper, we will introduce Power-Ground integrity, ad ...

9 Maximum voltage variation in the power distribution network of VLSI circuits with RLC model
Sudhakar Bobba, Ibrahim Hajj
August 2001 **Proceedings of the 2001 international symposium on Low power electronics an**

Full text available: pdf(245.18 KB) Additional Information: full citation, references, citings, index terms

10 Temperature-aware microarchitecture: Modeling and implementation
Kevin Skadron, Mircea R. Stan, Karthik Sankaranarayanan, Wei Huang, Sivakumar Velusamy, David
March 2004 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 1 Issue 1

Full text available: pdf(1.42 MB) Additional Information: full citation, abstract, references, citings, index term

With cooling costs rising exponentially, designing cooling solutions for worst-case power dissipatio prohibitively expensive. Chips that can autonomously modify their execution and power-dissipatio characteristics permit the use of lower-cost cooling solutions while still guaranteeing safe tempera regulation. Evaluating techniques for this *dynamic thermal management* (DTM), however, require model that is practical for architectural studies.This paper describes *HotSpo ...*

***Keywords**: Dynamic compact thermal models, dynamic thermal management, dynamic voltage s feedback control, fetch gating*

11 Power supply design parameters prediction for high performance IC design flows
M. Graziano, M. Delaurenti, M. Zamboni
April 2000 **Proceedings of the 2000 international workshop on System-level interconnect p**

Full text available: pdf(687.82 KB) Additional Information: full citation, references, citings, index terms

12 Decoupling capacitance allocation for power supply noise suppression
Shiyou Zhao, Kaushik Roy, Cheng-Kok Koh
April 2001 **Proceedings of the 2001 international symposium on Physical design**

Full text available: pdf(222.96 KB) Additional Information: full citation, abstract, references, citings, index term

We investigate the problem of decoupling capacitance allocation for power supply noise suppressio level. Decoupling capacitance budgets for the circuit modules are calculated based on the power s estimates. A linear programming technique is used to maximize the allocation of the existing whit floorplan for the placement of decoupling capacitors. An incremental heuristic is proposed to inser space into the existing floorplan to meet the rem ...

13 Mixed-signal design and simulation: Characterizing the effects of clock jitter due to substrate discrete-time D/S modulators
Payam Heydari
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(415.86 KB) Additional Information: full citation, abstract, references, index terms

This paper investigates the impact of clock jitter induced by substrate noise on the performance o oversampling DS modulators. First, a new stochastic model for substrate noise is proposed. This m utilized to study the clock jitter in clock generators incorporating phase-locked loops (PLLs). Next, the clock jitter on the performance of the DS modulator is studied. It will be shown that substrate degrades the signal-to-noise ratio of the DS modulator while the ...

Keywords: DS modulators, jitter, mixed-signal integrated circuits, phase noise, phase-locked loo noise

14 Power Grid and Signal Integrity Analysis: Scaling trends of on-chip Power distribution noise
Andrey V. Mezhiba, Eby G. Friedman
April 2002 **Proceedings of the 2002 international workshop on System-level interconnect p**

Full text available: pdf(110.79 KB) Additional Information: full citation, abstract, references, citings, index term

The design of power distribution networks in high performance integrated circuits has become sign challenging with recent advances in process technology. As on-chip currents exceed tens of ampe clock periods are reduced well below a nanosecond, the signal integrity of the on-chip power supp a primary concern in integrated circuit design. The existing work on power distribution noise scalin and extended to include the scaling of the inductanc ...

Keywords: power distribution, power supply noise, technology scaling

15 Session 10A: power analysis and optimization: Frequency domain analysis of switching nois supply network
Shiyou Zhao, Kaushik Roy, Cheng Kok Koh
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aid**

Full text available: pdf(224.20 KB) Additional Information: full citation, abstract, references, citings

In this paper, we propose an approach for the analysis of power supply noise in the frequency dom *power/ground* (P/G) networks of tree topologies. We model the P/G network as a linear time invar pseudo-distributed *RLC* network and the gates (or cells) as time-varying current sources. Voltage caused by the switching events is calculated based on the effective impedances seen by the corre current sources and the spatial correlation between the nodes ...

16 High-level simulation of substrate noise generation including power supply noise coupling
Marc van Heijningen, Mustafa Badaroglu, Stéphane Donnay, Marc Engels, Ivo Bolsens
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(114.20 KB) Additional Information: full citation, abstract, references, citings, index term

Substrate noise caused by large digital circuits will degrade the performance of analog circuits loc same substrate. To simulate this performance degradation, the total amount of generated substra be known. Simulating substrate noise generated by large digital circuits is however not feasible w circuit simulators and detailed substrate models due to the long simulation times and high memor requirements. We have developed a methodology to simulate this su ...

17 Advanced simulation and modeling techniques for hardware quality verification of digital syst
S. Forno, Stephen Rochel
September 1994 **Proceedings of the conference on European design automation**

Full text available: pdf(623.21 KB) Additional Information: full citation, references, citings, index terms

18 Temperature and power aware architectures: Pipeline muffling and a priori current ramping: techniques to reduce high-frequency inductive noise
Michael D. Powell, T. N. Vijaykumar
August 2003 **Proceedings of the 2003 international symposium on Low power electronics an**

Full text available: pdf(92.96 KB) Additional Information: full citation, abstract, references, index terms

While circuit and package designers have addressed microprocessor inductive noise issues in the p gigahertz clock frequencies and billion-transistor-level integration are exacerbating the problem, n microarchitectural solutions. The large net on-die decoupling capacitance used to address this nois the chip consumes substantial area and can cause a large leakage current. This paper proposes microarchitectural techniques to reduce high-frequency current variabilit ...

Keywords: a priori current ramping, decoupling capacitors, inductive noise, leakage, pipeline mu

19 Exploiting Resonant Behavior to Reduce Inductive Noise

June 2004 **Proceedings of the 31st annual international symposium on Computer architect Volume 00**

Full text available: pdf(190.42 KB) Publisher Site

Additional Information: full citation, abstract

Inductive noise in high-performance microprocessors is a reliabilityissue caused by variations in p current (di/dt)which are converted to supply-voltage glitches by impedances inthe power-supply n Inductive noise has been addressed byusing decoupling capacitors to maintain low impedance in t supply over a wide range of frequencies. However, evenwell-designed power supplies exhibit (a fe high impedanceat resonant frequencies caused by RLC resonant loops. Previousa ...

20 Layout tools for analog ICs and mixed-signal SoCs: a survey

Rob A. Rutenbar, John M. Cohn

May 2000 **Proceedings of the 2000 international symposium on Physical design**

Full text available: pdf(247.03 KB) Additional Information: full citation, references

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Terms used
power distribution and **decoupling capacitors** and **simulation** and **model** and **impedance** and **rung**

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1 Session 10C: Embedded tutorial: IC power distribution challenges: IC power distribution challenges
Sudhakar Bobba, Tyler Thorp, Kathirgamar Aingaran, Dean Liu
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(125.96 KB) Additional Information: full citation, abstract, references, citings, index terms

With each technology generation, delivering a timevarying current with reduced nominal supply voltage variation is becoming more difficult due to increasing current and power requirements. The power delivery network design becomes much more complex and requires accurate analysis and optimizations at all levels of abstraction in order to meet the specifications. In this paper, we describe techniques for estimation of the supply voltage variations that can be used in the design of the power delive ...

2 Power distribution issues: Macro-modeling concepts for the chip electrical interface
Brian W. Amick, Claude R. Gauthier, Dean Liu
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(515.95 KB) Additional Information: full citation, abstract, references, index terms

The power delivery network is made up of passive elements in the distribution network, as well as the active transistor loads. A chip typically has three types of power supplies that require attention: core, I/O, and analog. Core circuits consist of digital circuits and have the largest current demand. In addition to all of the system issues/models for the core, modeling the I/O subsystem has the additional requirement of modeling return paths and discontinuities. The analog circuits present yet ...

Keywords: VLSI power distribution, analog and I/O power delivery, high speed microprocessor design, inductance

3 Session 10A: power analysis and optimization: Simulation and optimization of the power distribution network in VLSI circuits
G. Bai, S. Bobba, I. N. Hajj
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings

In this paper, we present simulation techniques to estimate the worst-case voltage variation using a RC model for the power distribution network. Pattern independent maximum envelope currents are used as a periodic input for performing the frequency-domain steady-state simulation of the linear RC circuit to evaluate the worst-case instantaneous voltage drop for the RC power distribution networks. The proposed technique unlike existing techniques, is guaranteed to give the maximum voltage drop at ...

4 Modeling of Multi-Layered Power Distribution Planes Including Via Effects Using Transmission Matrix Method

Joong-Ho Kim, Erdem Matoglu, Jinwoo Choi, Madhavan Swaminathan

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(259.07 KB) Publisher Site

Additional Information: full citation, abstract

This paper presents a method for analyzing multi-layered power distribution networks in the frequency domain.Using a two dimensional array of distributed RLCG circuits,multi-layered power distribution planes are represented.Each plane pair is connected by vias, which are modeled as partial self and mutual inductors. For the efficient computation of the power distribution impedances at specific points in the network,a multi-input and multi-output transmission matrix method has been used, which is ...

5 Electromagnetic modeling and signal integrity simulation of power/ground networks in high speed digital packages and printed circuit boards

Frank Y. Yuan

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(275.46 KB) Publisher Site

Additional Information: full citation, abstract, references, index terms

The electromagnetic modeling and parameter extraction of digital packages and PCB boards for system signal integrity applications are presented. A systematic approach to analyze complex power/ground structures and simulate their effects on digital systems is developed. First, an integral equation boundary element algorithm is applied to the electromagnetic modeling of the PCB structures. Then, equivalent circuits of the power/ground networks are extracted from the EM solution. In an integra ...

Keywords: custom sizing, migration, timing optimazation

6 Interconnect parasitic extraction in the digital IC design methodology

Mattan Kamon, Steve McCormick, Ken Sheperd

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(129.08 KB)

Additional Information: full citation, abstract, references, citings, index terms

Accurate interconnect analysis has become essential not only for post-layout verification but also for synthesis. This tutorial explores interconnect analysis and extraction methodology on three levels: coarse extraction to guide synthesis, detailed extraction for full-chip analysis, and full 3D analysis for critical nets. We will also describe the electrical issues caused by parasitics and how they have, and will be, influenced by changing technology. The importance of model order ...

7 Power supply noise analysis methodology for deep-submicron VLSI chip design

Howard H. Chen, David D. Ling

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available:

pdf(237.07 KB) Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

This paper describes a new design methodology to analyzethe on-chip power supply noise for high-performance microprocessors.Based on an integrated package-level andchip-level power bus model, and a simulated switching circuitmodel for each functional block, this methodology offersthe most complete and accurate analysis of Vdd distributionfor the entire chip. The analysis results not only providedesigners with the inductive ¿I noise and the resistive IRdrop data at the same time, but also allow d ...

8 Session 1OC: Embedded tutorial: IC power distribution challenges: Challenges in power-ground integrity

Shen Lin, Norman Chang

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(54.74 KB) Additional Information: full citation, abstract, references, citings, index terms

With the advance of semiconductor manufacturing, EDA, and VLSI design technologies, circuits with increasingly higher speed are being integrated at an increasingly higher density. This trend causes correspondingly larger voltage fluctuations in the on-chip power distribution network due to IR-drop, L di/dt noise, or LC resonance. Therefore, Power-Ground integrity becomes a serious challenge in designing future high-performance circuits. In this paper, we will introduce Power-Ground integrity, ad ...

9 Decoupling capacitance allocation for power supply noise suppression

Shiyou Zhao, Kaushik Roy, Cheng-Kok Koh

April 2001 **Proceedings of the 2001 international symposium on Physical design**

Full text available: pdf(222.96 KB) Additional Information: full citation, abstract, references, citings, index terms

We investigate the problem of decoupling capacitance allocation for power supply noise suppression at floorplan level. Decoupling capacitance budgets for the circuit modules are calculated based on the power supply noise estimates. A linear programming technique is used to maximize the allocation of the existing white space in the floorplan for the placement of decoupling capacitors. An incremental heuristic is proposed to insert more white space into the existing floorplan to meet the rem ...

10 Maximum voltage variation in the power distribution network of VLSI circuits with RLC models

Sudhakar Bobba, Ibrahim Hajj

August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

Full text available: pdf(245.18 KB) Additional Information: full citation, references, citings, index terms

11 Power Grid and Signal Integrity Analysis: Scaling trends of on-chip Power distribution noise

Andrey V. Mezhiba, Eby G. Friedman

April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction**

Full text available: pdf(110.79 KB) Additional Information: full citation, abstract, references, citings, index terms

The design of power distribution networks in high performance integrated circuits has become significantly more challenging with recent advances in process technology. As on-chip currents exceed tens of amperes and circuit clock periods are reduced well below a nanosecond, the signal integrity of the on-chip power supply has become a primary concern in integrated circuit design. The existing work on power distribution noise scaling is

reviewed and extended to include the scaling of the inductanc ...

Keywords: power distribution, power supply noise, technology scaling

12 Session 10A: power analysis and optimization: Frequency domain analysis of switching noise on power supply network

Shiyou Zhao, Kaushik Roy, Cheng Kok Koh

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(224.20 KB) Additional Information: full citation, abstract, references, citings

In this paper, we propose an approach for the analysis of power supply noise in the frequency domain for *power/ground* (P/G) networks of tree topologies. We model the P/G network as a linear time invariant (LTI) pseudo-distributed *RLC* network and the gates (or cells) as time-varying current sources. Voltage fluctuation caused by the switching events is calculated based on the effective impedances seen by the corresponding current sources and the spatial correlation between the nodes ...

13 High-level simulation of substrate noise generation including power supply noise coupling

Marc van Heijningen, Mustafa Badaroglu, Stéphane Donnay, Marc Engels, Ivo Bolsens

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(114.20 KB) Additional Information: full citation, abstract, references, citings, index terms

Substrate noise caused by large digital circuits will degrade the performance of analog circuits located on the same substrate. To simulate this performance degradation, the total amount of generated substrate noise must be known. Simulating substrate noise generated by large digital circuits is however not feasible with existing circuit simulators and detailed substrate models due to the long simulation times and high memory requirements. We have developed a methodology to simulate this su ...

14 Power supply design parameters prediction for high performance IC design flows

M. Graziano, M. Delaurenti, M. Zamboni

April 2000 **Proceedings of the 2000 international workshop on System-level interconnect prediction**

Full text available: pdf(687.82 KB) Additional Information: full citation, references, citings, index terms

15 Temperature and power aware architectures: Pipeline muffling and a priori current ramping: architectural techniques to reduce high-frequency inductive noise

Michael D. Powell, T. N. Vijaykumar

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(92.96 KB) Additional Information: full citation, abstract, references, index terms

While circuit and package designers have addressed microprocessor inductive noise issues in the past, multi-gigahertz clock frequencies and billion-transistor-level integration are exacerbating the problem, necessitating microarchitectural solutions. The large net on-die decoupling capacitance used to address this noise throughout the chip consumes substantial area and can cause a large leakage current. This paper proposes microarchitectural techniques to reduce high-frequency current variabilit ...

Keywords: a priori current ramping, decoupling capacitors, inductive noise, leakage, pipeline muffling

16 Mixed-signal design and simulation: Characterizing the effects of clock jitter due to substrate noise in discrete-time D/S modulators

Payam Heydari

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(415.86 KB) Additional Information: full citation, abstract, references, index terms

This paper investigates the impact of clock jitter induced by substrate noise on the performance of the oversampling DS modulators. First, a new stochastic model for substrate noise is proposed. This model is then utilized to study the clock jitter in clock generators incorporating phase-locked loops (PLLs). Next, the effect of the clock jitter on the performance of the DS modulator is studied. It will be shown that substrate noise degrades the signal-to-noise ratio of the DS modulator while the ...

Keywords: DS modulators, jitter, mixed-signal integrated circuits, phase noise, phase-locked loop, substrate noise

17 Implicit treatment of substrate and power-ground losses in return-limited inductance extraction

Dipak Sitaram, Yu Zheng, K. L. Shepard

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(192.35 KB) Additional Information: full citation, abstract, references, index terms

Full-wave analysis, based on rigorous solution of the differential or integral form of Maxwell's equations, is too slow for all but the smallest designs. Traditional on-chip extraction engines are, therefore, being pushed to extract inductance and provide accurate high-frequency interconnect modelling while maintaining computational efficiency and capacity. This paper describes further accuracy-improving enhancements to the commecial full-chip RLCK extraction engine, Assura RLCX[1], based on the ...

18 Temperature-aware microarchitecture: Modeling and implementation

Kevin Skadron, Mircea R. Stan, Karthik Sankaranarayanan, Wei Huang, Sivakumar Velusamy, David Tarjan

March 2004 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 1 Issue 1

Full text available: pdf(1.42 MB) Additional Information: full citation, abstract, references, citings, index terms

With cooling costs rising exponentially, designing cooling solutions for worst-case power dissipation is prohibitively expensive. Chips that can autonomously modify their execution and power-dissipation characteristics permit the use of lower-cost cooling solutions while still guaranteeing safe temperature regulation. Evaluating techniques for this *dynamic thermal management* (DTM), however, requires a thermal model that is practical for architectural studies.This paper describes *HotSpo* ...

***Keywords**: Dynamic compact thermal models, dynamic thermal management, dynamic voltage scaling, feedback control, fetch gating*

19 Exploiting Resonant Behavior to Reduce Inductive Noise

June 2004 **Proceedings of the 31st annual international symposium on Computer architecture - Volume 00**

Full text available: pdf(190.42 KB) Publisher Site Additional Information: full citation, abstract

Inductive noise in high-performance microprocessors is a reliabilityissue caused by variations in processor current (di/dt)which are converted to supply-voltage glitches by impedances inthe power-supply network. Inductive noise has been addressed byusing decoupling capacitors to maintain low impedance in thepower supply over a wide range of

frequencies. However, evenwell-designed power supplies exhibit (a few) peaks of high impedanceat resonant frequencies caused by RLC resonant loops. Previousa ...

20 Power Supply Noise Aware Floorplanning and Decoupling Capacitance Placement

Shiyou Zhao, Kaushik oy, Cheng-Kok Koh

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(217.57 KB) Publisher Site

Additional Information: full citation, abstract

Power supply noise is strong function of the switching activities of the circuit modules. Peak power supply noise can be significantly reduced by judiciously arranging the modules based on their spatial correlations in the floorplan. In this paper, power supply noise is, for the first time, incorporated into the cost function to determine the optimal floorplan in terms of real, wire length, and power supply noise. Compared to the conventional floorplanning which only considers area and wire leng ...

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1 Session 10C: Embedded tutorial: IC power distribution challenges: IC power distribution challenges
Sudhakar Bobba, Tyler Thorp, Kathirgamar Aingaran, Dean Liu
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(125.96 KB) Additional Information: full citation, abstract, references, citings, index terms

With each technology generation, delivering a timevarying current with reduced nominal supply voltage variation is becoming more difficult due to increasing current and power requirements. The power delivery network design becomes much more complex and requires accurate analysis and optimizations at all levels of abstraction in order to meet the specifications. In this paper, we describe techniques for estimation of the supply voltage variations that can be used in the design of the power delive ...

2 Power distribution issues: Macro-modeling concepts for the chip electrical interface
Brian W. Amick, Claude R. Gauthier, Dean Liu
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(515.95 KB) Additional Information: full citation, abstract, references, index terms

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Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings

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August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

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Keywords: power distribution, power supply noise, technology scaling

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Shiyou Zhao, Kaushik Roy, Cheng Kok Koh

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Michael D. Powell, T. N. Vijaykumar

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Payam Heydari

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Keywords: DS modulators, jitter, mixed-signal integrated circuits, phase noise, phase-locked loop, substrate noise

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Dipak Sitaram, Yu Zheng, K. L. Shepard

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Full text available: pdf(190.42 KB) Publisher Site Additional Information: full citation, abstract

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19 Advanced simulation and modeling techniques for hardware quality verification of digital systems

S. Forno, Stephen Rochel

September 1994 **Proceedings of the conference on European design automation**

Full text available: pdf(623.21 KB) Additional Information: full citation, references, citings, index terms

20 Layout tools for analog ICs and mixed-signal SoCs: a survey

Rob A. Rutenbar, John M. Cohn

May 2000 **Proceedings of the 2000 international symposium on Physical design**

Full text available: pdf(247.03 KB) Additional Information: full citation, references

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L6: Entry 1 of 8 File: PGPB May 6, 2004

PGPUB-DOCUMENT-NUMBER: 20040088661
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040088661 A1

TITLE: Methodology for determining the placement of decoupling capacitors in a power distribution system

PUBLICATION-DATE: May 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Anderson, Raymond E.	Santa Cruz	CA	US	
Smith, Larry D.	San Jose	CA	US	
Chun, Sungjun	Austin	TX	US	

US-CL-CURRENT: 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. D

☐ 2. Document ID: US 20030021136 A1

L6: Entry 2 of 8 File: PGPB Jan 30, 2003

PGPUB-DOCUMENT-NUMBER: 20030021136
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030021136 A1

TITLE: 256 Meg dynamic random access memory

PUBLICATION-DATE: January 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Keeth, Brent	Boise	ID	US	
Bunker, Layne G.	Boise	ID	US	
Demer, Scott J.	Meridian	ID	US	
Taylor, Ronald L.	Meridian	ID	US	
Mullin, John S.	Boise	ID	US	
Beffa, Raymond J.	Boise	ID	US	

Ross, Frank F.	Boise	ID	US
Kinsman, Larry D.	Boise	ID	US

US-CL-CURRENT: 365/51; 257/E27.085

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 3. Document ID: US 20020172007 A1

L6: Entry 3 of 8 File: PGPB Nov 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020172007
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020172007 A1

TITLE: Spray evaporative cooling system and method

PUBLICATION-DATE: November 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Pautsch, Gregory W.	Chippewa Falls	WI	US	

US-CL-CURRENT: 361/690; 165/908, 257/E23.1, 62/259.2

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 20020169590 A1

L6: Entry 4 of 8 File: PGPB Nov 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020169590
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020169590 A1

TITLE: System and method for determining the required decoupling capacitors for a power distribution system using an improved capacitor model

PUBLICATION-DATE: November 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Smith, Larry D.	San Jose	CA	US	
Hockanson, David	Boulder Creek	CA	US	

US-CL-CURRENT: 703/18

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 20020135981 A1

L6: Entry 5 of 8 File: PGPB Sep 26, 2002

PGPUB-DOCUMENT-NUMBER: 20020135981
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020135981 A1

TITLE: Method and apparatus for cooling electronic components

PUBLICATION-DATE: September 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Pautsch, Gregory W.	Chippewa Falls	WI	US	

US-CL-CURRENT: 361/700; 165/104.33, 257/714, 257/E23.1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 6. Document ID: US 20020011894 A1

L6: Entry 6 of 8 File: PGPB Jan 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020011894
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020011894 A1

TITLE: 256 Meg dynamic random access memory

PUBLICATION-DATE: January 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Keeth, Brent	Boise	ID	US	
Bunker, Layne G.	Boise	ID	US	
Derner, Scott J.	Meridian	ID	US	

US-CL-CURRENT: 327/536; 257/E27.085

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 7. Document ID: US 6646879 B2

L6: Entry 7 of 8 File: USPT Nov 11, 2003

US-PAT-NO: 6646879
DOCUMENT-IDENTIFIER: US 6646879 B2
**** See image for Certificate of Correction ****

TITLE: Spray evaporative cooling system and method

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY

Pautsch; Gregory W. Chippewa Falls WI

US-CL-CURRENT: 361/699; 165/104.33, 165/80.4, 174/15.1, 257/E23.1, 361/689, 361/698, 361/700, 361/701, 361/704, 62/259.2 , 62/64

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 8. Document ID: US 6580609 B2

L6: Entry 8 of 8 File: USPT Jun 17, 2003

US-PAT-NO: 6580609
DOCUMENT-IDENTIFIER: US 6580609 B2

TITLE: Method and apparatus for cooling electronic components

DATE-ISSUED: June 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pautsch; Gregory W.	Chippewa Falls	WI		

US-CL-CURRENT: 361/698; 165/80.4, 257/714, 257/E23.1, 29/890.03, 361/700, 62/259.2

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

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RAILS	127284
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(L4 AND RAIL).PGPB,USPT.	8

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Search Results - Record(s) 1 through 2 of 2 returned.

No ☐ 1. Document ID: US 20040088661 A1

Using default format because multiple data bases are involved.

L5: Entry 1 of 2 File: PGPB May 6, 2004

PGPUB-DOCUMENT-NUMBER: 20040088661
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040088661 A1

TITLE: Methodology for determining the placement of decoupling capacitors in a power distribution system

PUBLICATION-DATE: May 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Anderson, Raymond E.	Santa Cruz	CA	US	
Smith, Larry D.	San Jose	CA	US	
Chun, Sungjun	Austin	TX	US	

US-CL-CURRENT: 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 2. Document ID: US 20020169590 A1

L5: Entry 2 of 2 File: PGPB Nov 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020169590
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020169590 A1

TITLE: System and method for determining the required decoupling capacitors for a power distribution system using an improved capacitor model

PUBLICATION-DATE: November 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Smith, Larry D.	San Jose	CA	US	
Hockanson, David	Boulder Creek	CA	US	

US-CL-CURRENT: 703/18

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D